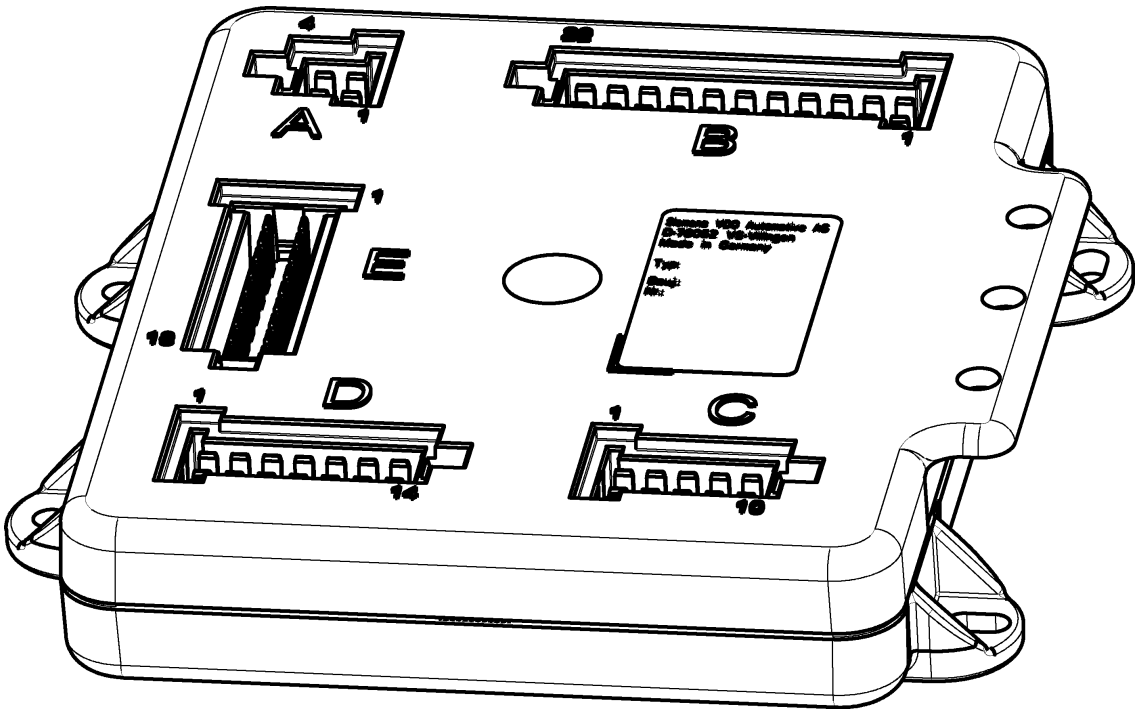


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Multiplex Node MUX2-M

Hardware Documentation

From version 3.0



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2 Revision index

2.1 History

Version	Date	Revision	Name
00.01.00	09.12.96	Initial version	T. Schupp
00.02.00	02.07.97	Housing material and dimensions Name change from MUX to MUX2-M	T. Schupp
00.03.00	15.07.97	Amendments under tech. data / scope	T. Schupp
00.04.00	17.03.98	New : 14HSS, 2LSS	T. Schupp
00.05.00	23.06.98	More details pertaining to the specification "reverse battery protection"	T. Schupp
00.06.00	11.12.98	More details pertaining to the specification LSS with PWM Description of half-bridges extended Description of EIN_STATUS extended Description of EIN_ANALOG extended	T. Schupp
01.00.00	14.05.02	Printed circuit board redesign, SW revision: latching behavior of the HSS and delayed activation of LSS. Version MUX2-M up-graded to V0.3 (rating plate).	R. Christein
01.01.00	09.09.02	Additional description of the necessary circuit protection of the LS-loads	R. Christein

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2.2 Summary of the important modifications starting from version 3.0 of MUX2-B

- Improved load-dump protection; suited for operation without central load-dump protection.
- Slightly modified switch-on behavior of low-side switch.
- Modifications regarding the high-side switches:
 - Lower currents with short circuit to ground
 - Better protection in case of short circuit because the HSS is not automatically switched on after cooling down (overload latch). Same behavior as with LSS.
 - For the open-load recognition, a pull-up resistors of 330kΩ per output pin (typ. 80μA with 24V mode) is used instead of a current source (typ. 30...60μA / 3A channel). The resistors are switched off in the stand-by mode.
 - When the HSS is in on-position, the output is no longer switched off in case of overvoltage (so far at 34-43V). In case of voltages higher than the typical 47V, the output is on the difference voltage (PLUS_Gx – 47V) as usual.
 - Reduced E_{AS} values are applicable for switching off of inductive loads

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3 Introduction

3.1 Terms

KIBES-2 Key to on Board Electronic Systems
second generation

DWP (or FAP) Driver Work Place by Siemens VDO
(German: **F**ahrer-**A**rbeits-**P**latz)

3.2 Acronyms

ADC Analog digital converter

ZR2 Central computer 2 (German: **Z**entral **R**echner)

MUX2 MultipleX node for ZR2

EOL End Of Line Programming

HB Half bridge
HS High side
HSS High side switch

LS Low side
LSS Low side switch

PLC Programmable Logic Control (German: SPS)

GND **G**round, battery minus

CAN Controller Area Network

PCAN Powertrain CAN

ICAN Instrumentation CAN

KCAN Body CAN

MCAN Multiplex CAN

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4 Scope

The distributed multiplex system consists of a central computer and several multiplex nodes, which can be split to 2 multiplex branches.

Restrictions

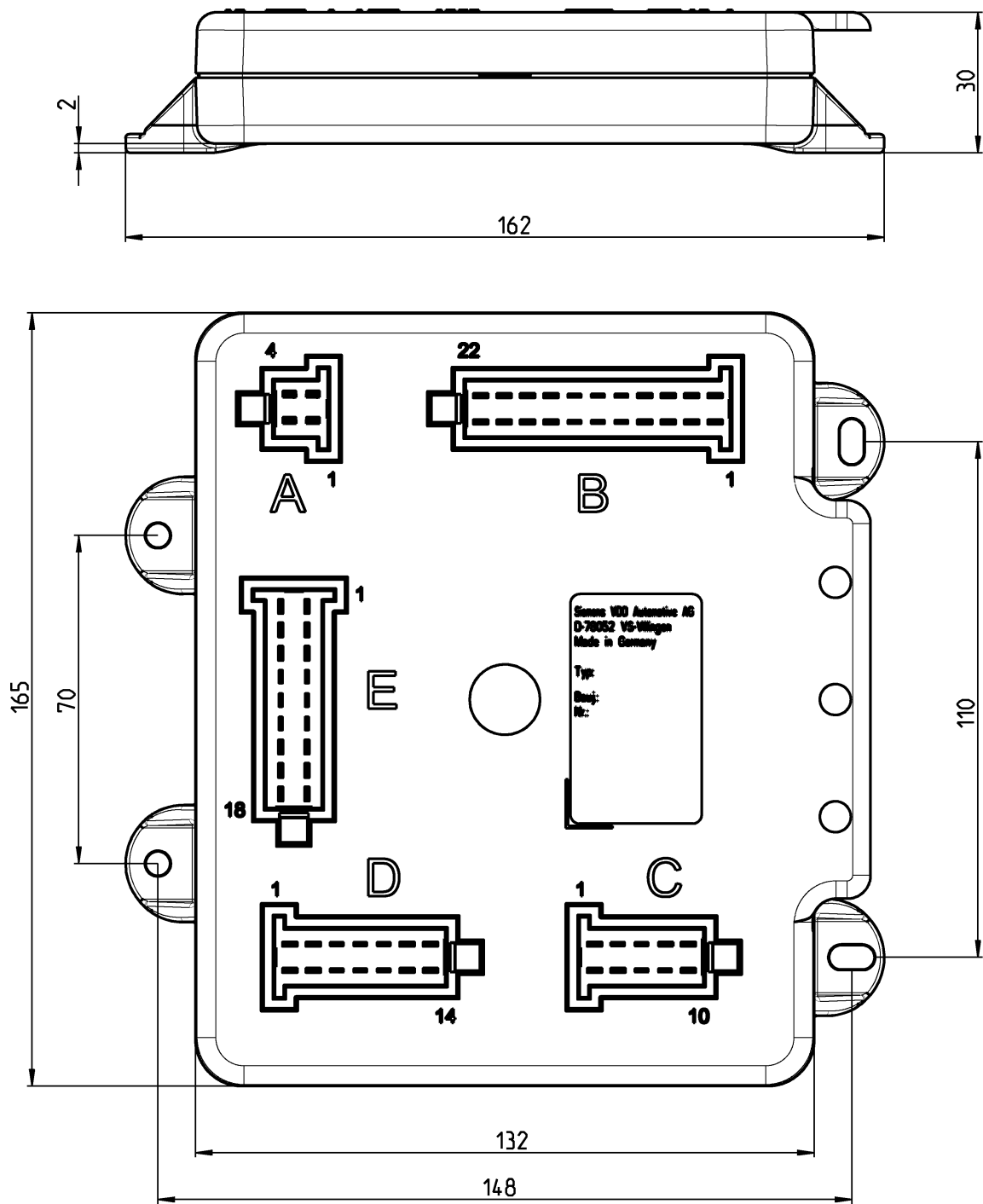
- KIBES is not designed to control safety related systems.
- There is no approval available for the operation in explosion areas.
- Assembly or connection of KIBES components while operating voltage is connected is not admitted.

4.1 Technical system structure

See HW documentation of the relevant central computer.

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4.2 Housing



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4.3 Connector assignment

E

AUS_16_G2_HS	17	18	MINUS_G2
AUS_15_G2_HS	15	16	MINUS_G2
AUS_14_G2_HS	13	14	MINUS_G2
AUS_13_G2_HS	11	12	MINUS_G2
	9	10	MINUS_G2
AUS_12_G2_HS	7	8	MINUS_G2
AUS_11_G2_HS	5	6	MINUS_G2
AUS_10_G2_HS	3	4	MINUS_G2
AUS_09_G2_HS	1	2	MINUS_G2

D

EIN_STATUS_02	2	1	EIN_STATUS_01
EIN_STATUS_04	4	3	EIN_STATUS_03
EIN_STATUS_06	6	5	EIN_STATUS_05
EIN_STATUS_08	8	7	EIN_STATUS_07
EIN_STATUS_10	10	9	EIN_STATUS_09
EIN_STATUS_12	12	11	EIN_STATUS_11
EIN_ANALOG_02	14	13	EIN_ANALOG_01

A

PLUS_G2	3	4	MINUS_G2
PLUS_G1	1	2	MINUS_G1

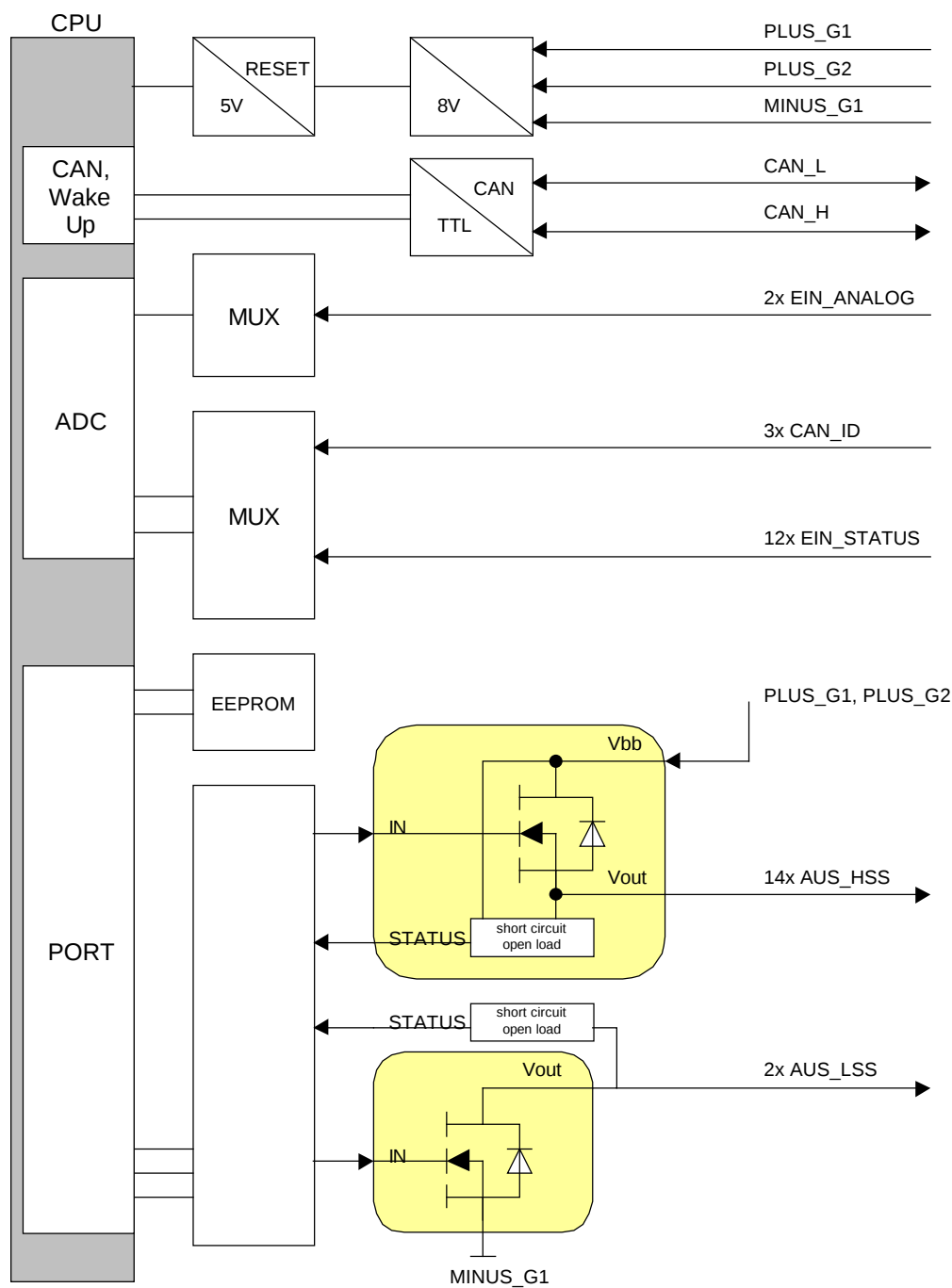
B

AUS_01_G1_HS	21	22	MINUS_G1
AUS_02_G1_HS	19	20	MINUS_G1
	17	18	MINUS_G1
AUS_03_G1_HS	15	16	MINUS_G1
AUS_04_G1_HS	13	14	MINUS_G1
	11	12	MINUS_G1
AUS_05_G1_HS	9	10	MINUS_G1
AUS_06_G1_HS	7	8	MINUS_G1
	5	6	MINUS_G1
AUS_07_G1_LS	3	4	MINUS_G1
AUS_08_G1_LS	1	2	MINUS_G1

C

CAN_H1	2	1	CAN_L1
CAN_H2	4	3	CAN_L2
EIN_ID_01	6	5	CAN_L_ABSCHL
EIN_ID_03	8	7	EIN_ID_02
AUS_ID_PLUS	10	9	AUS_ID_MINUS

4.4 Block circuit diagram



4.5 Supply voltage

The system is supplied by constant power supply. It is awakened through activities at the CAN-Bus (by the central computer ZR2).

4.6 Computer core

The computer core consists of an 8-bit microprocessor with peripheral extensions. The program is located in a read only memory (ROM).

4.7 Inputs and outputs

4.7.1 Inputs

- 12 quasi-analog status inputs
- 2 analog inputs
- 3 unit address bits (unit number 1...8)

4.7.2 Outputs

The outputs are split into 2 groups, which are supplied with separate external voltage supplies. Each of these voltage supplies has to have a fuse protection of a maximum of 15A.

4.7.2.1 High side outputs

- 14 HIGHSIDE switches with 3A each

4.7.2.2 Low side outputs

- 2 LOWSIDE switches with 3A each

4.8 Interfaces

- 1 CAN according to ISO 11898 to the central computer, wakeup capable.
Point to point connection to the central computer and other multiplex nodes.
Signals on the CAN awaken the system (wakeup capable).

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4.9 Firmware

The multiplex node is controlled by a processor with its own program, which can not be changed by the user. The central computer ZR2 controls the complete system. For the INPUTS and OUTPUTS, individual parameters can be selected in the allocation editor of the PLC program.

Initialization of the multiplex nodes

When starting the system the central computer ZR2 executes a self-test of the system. All connected multiplex nodes are checked for a valid allocation code. Multiplex nodes that do not function are reported to the PLC and eliminated from the current processing. If the ZR2 recognizes a new or exchanged multiplex node during the self-test (unknown allocation code), then a new distinctive code is generated for this multiplex node and stored together with the „fail safe“ operation parameters defined in the PLC program in the EEPROM of the multiplex node.

An inadmissible exchange of the multiplex node while the system is running causes the multiplex nodes to be turned off with unknown allocation code. A new initialization with the defined „fail safe“ operation parameters and a new allocation code takes place at the next system start.

If a multiplex node defined via allocation code is missing, it is reported to the PLC program. The ZR2 tries cyclically to contact this multiplex node.

If this happens during the operating phase, then the error code is reset and the multiplex node is integrated again into the normal process.

Characteristics of a multiplex node in case of an error

If the multiplex node does not establish a connection to the ZR2 during the self-test, then all outputs are switched to logically inactive.

If a multiplex node detects a missing connection to the ZR2 during operation, then it switches in the „fail safe“ operation mode. The outputs of the multiplex node are switched as defined in the „fail safe“ operation parameters that can be programmed in the PLC program and as stored during the initialization.

The status of the outputs during „fail safe“ operation can be programmed as follows:

- output turned off
- output turned on
- output is kept in the last logic status
- output flashes

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5 Technical data

5.1 Scope

Operational temperature	:	-30°C ... +80°C	at partial load (80%)
		-30°C ... +70°C	at full load
Storage temperature	:	-40°C ... +90°C	
Protection type	:	IP40 with connected plugs	

To protect the unit and the wire harness (contacts), assembly and disassembly may only be done with power disconnected.

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5.2 Current supply

	Name	Connector pin
Group 1	PLUS_G1	A1
	MINUS_G1	A2
Group 2	PLUS_G2	A3
	MINUS_G2	A4

The multiplex node logic system is supplied via PLUS_G1 or PLUS_G2 and MINUS_G1.

Note: MINUS_G1 and MINUS_G2 are not connected internally.

Nominal voltages	12 V	
	24 V	
Functional range	8V - 16V	
	16 V - 32 V	
	36 V for 1h at a max. of 40°C environmental temperature	
Operational voltage	40mA / 12V	PLUS_G1, PLUS_G2, MINUS_G1
	60mA / 24V	
Stand-by current	2.0mA / 12V	PLUS_G1,2
	2.5mA / 24V	

5.3 Unit activation

The multiplex node is activated through an incoming CAN message (wake-up).

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5.4 Interfaces

5.4.1 CAN to the central computer (MCAN)

Name	Connector pin
CAN_L1	C1
CAN_H1	C2
CAN_L2	C3
CAN_H2	C4
CAN_L_ABSCHL	C5

The connector pins with the names CAN_L1 and CAN_L2, as well as CAN_H1 and CAN_H2 are connected internally and therefore equivalent.
This is valid for multiplex node and central computer.

CAN according to ISO 11898, baud rate 125 kBaud, wakeup capable.

* CAN termination resistance

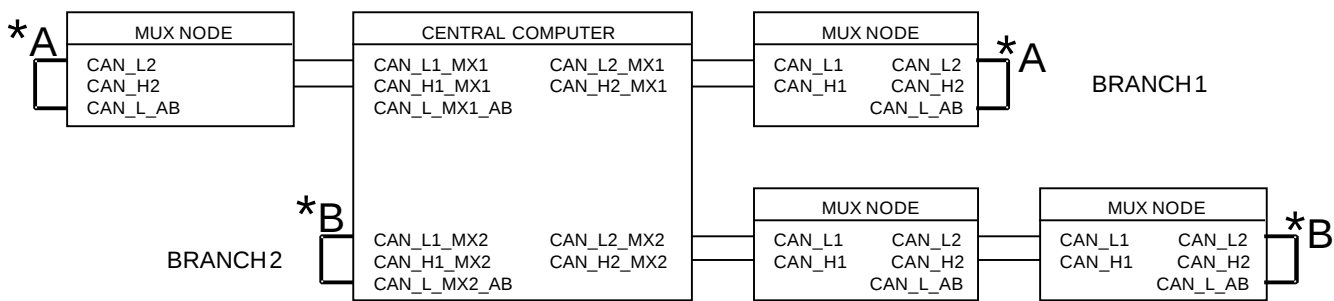
The following note refers to the block circuit diagrams on the following page.

The necessary CAN termination resistance at the first and the last unit exists inside each multiplex node and in the central computer ZR2. It is activated via a jumper (*) at the respective end of the branch. Both ends of a branch have to be terminated with a resistor.

***A** The CAN termination resistance is activated at the first and last multiplex node in the branch.

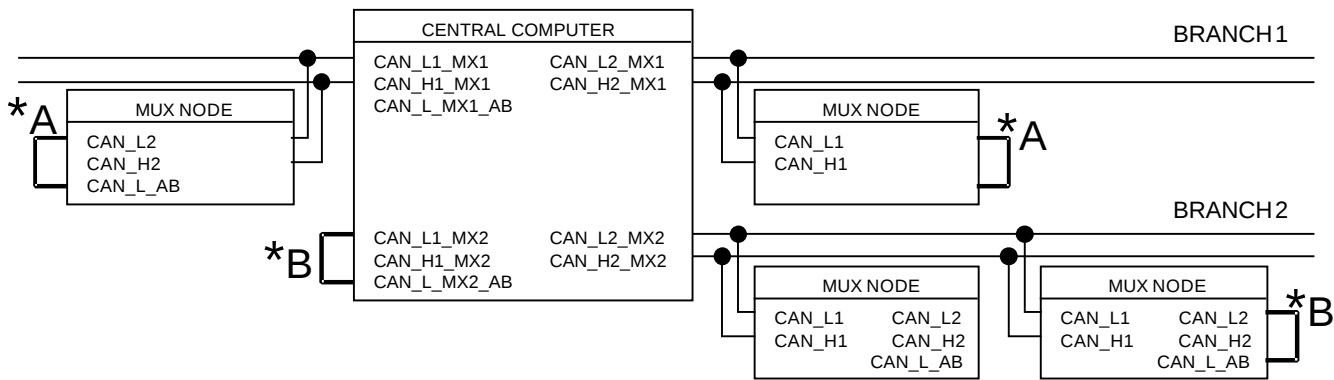
***B** The CAN termination resistance is activated at the central computer and at the last multiplex node.

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Note: If a multiplex node is removed from the center of the branch on this connection diagram, all following multiplex nodes are separated from the branch (CAN bridge is located in the multiplex node).
The central computer recognizes a defective or non-existent multiplex node. The message can be evaluated via the PLC program.

Through the integration of a “T- piece” in the wire harness this connection diagram can be realized, in which a removal of a multiplex node does not have any influence on the other components of the branch.



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5.4.2 Unit number (ID)

Name	Connector pin
EIN_ID_01	C6
EIN_ID_02	C7
EIN_ID_03	C8
AUS_ID_MINUS	C9
AUS_ID_PLUS	C10

The unit number (1..8) is specified via the unit address bits EIN_ID_01, EIN_ID_02 and EIN_ID_03.

The unit address bits are detected via analog signals and are internally diagnosis capable. A contact current of about 5mA against AUS_ID_PLUS or AUS_ID_MINUS is provided.

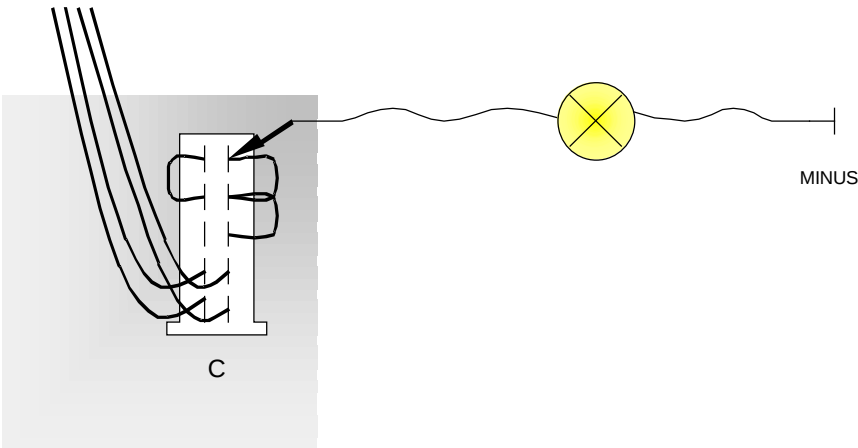
Unit No.	EIN_ID_03	EIN_ID_02	EIN_ID_01
1	AUS_ID_MINUS	AUS_ID_MINUS	AUS_ID_MINUS
*) 2	AUS_ID_MINUS	AUS_ID_MINUS	AUS_ID_PLUS
3	AUS_ID_MINUS	AUS_ID_PLUS	AUS_ID_MINUS
4	AUS_ID_MINUS	AUS_ID_PLUS	AUS_ID_PLUS
5	AUS_ID_PLUS	AUS_ID_MINUS	AUS_ID_MINUS
6	AUS_ID_PLUS	AUS_ID_MINUS	AUS_ID_PLUS
7	AUS_ID_PLUS	AUS_ID_PLUS	AUS_ID_MINUS
8	AUS_ID_PLUS	AUS_ID_PLUS	AUS_ID_PLUS

*) Example: In order to set the unit number 2, jumpers have to be placed on the connector from AUS_ID_MINUS to EIN_ID_03 and EIN_ID_02, as well as from AUS_ID_PLUS to EIN_ID_01.

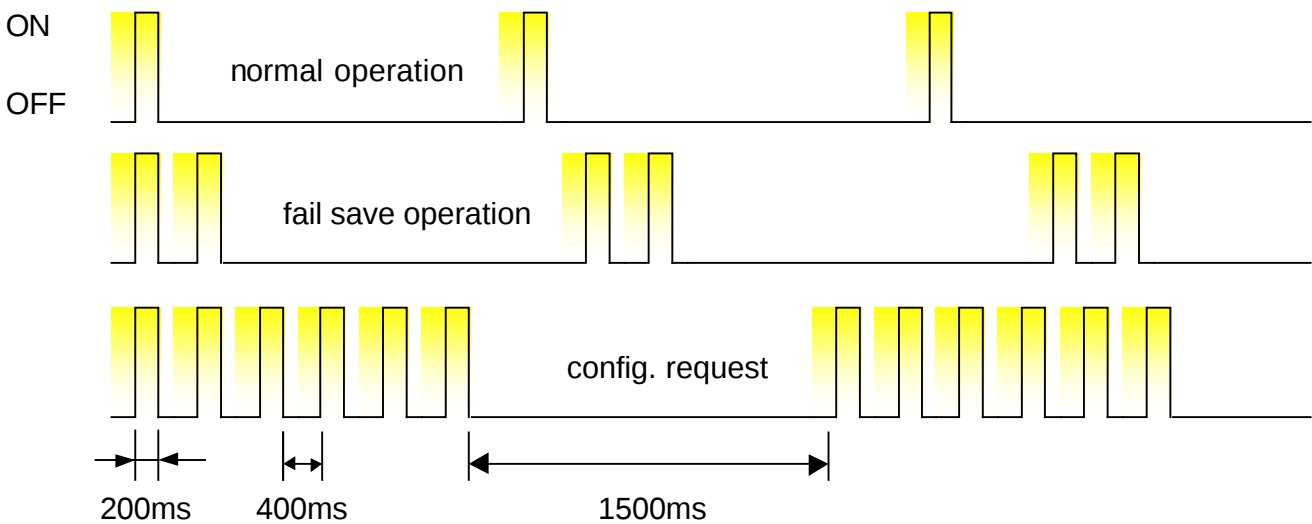
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5.4.2.1 External node diagnosis

To AUS_ID_PLUS, a 2W bulb in connection with a 24V power supply (or 1W with 12V power supply) can be connected for functional checks.



Error conditions	Cause of the failure
„FAIL SAFE“ OPERATION	CAN – connection failed during operation
CONFIGURATION REQUEST	Incorrect node - ID, incorrect node type (MUX2-N,M,B) or new node (node not yet programmed→short term only, until programming is completed)
OFF	Voltage supply or CAN already defective or not present when turning on or node defective
ON	Node defective, voltage supply O.K.



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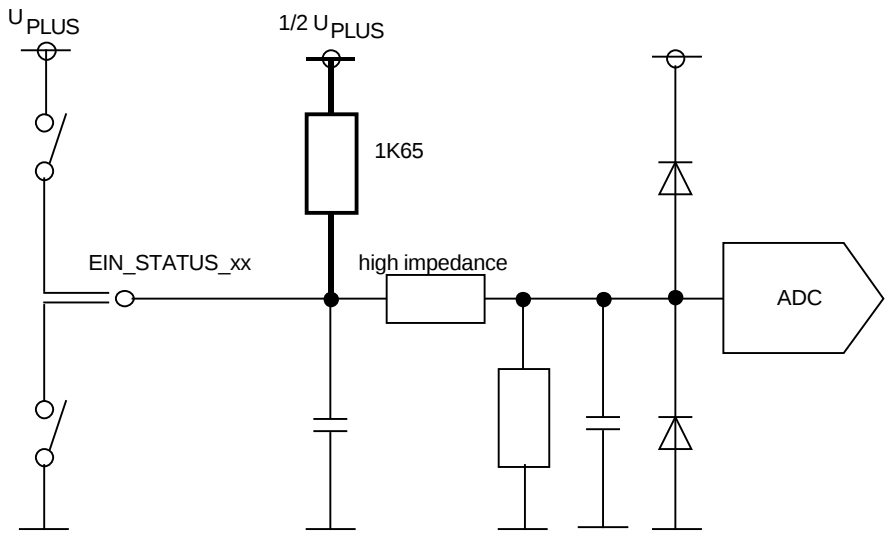
5.5 Inputs and outputs

5.5.1 Inputs

5.5.1.1 Status inputs

Name	Connector pin	Contact current at $U_N = 24V$	Contact current at $U_N = 12V$
EIN_STATUS_01	D1	7mA	3.5mA
EIN_STATUS_02	D2	7mA	3.5mA
EIN_STATUS_03	D3	7mA	3.5mA
EIN_STATUS_04	D4	7mA	3.5mA
EIN_STATUS_05	D5	7mA	3.5mA
EIN_STATUS_06	D6	7mA	3.5mA
EIN_STATUS_07	D7	7mA	3.5mA
EIN_STATUS_08	D8	7mA	3.5mA
EIN_STATUS_09	D9	7mA	3.5mA
EIN_STATUS_10	D10	7mA	3.5mA
EIN_STATUS_11	D11	7mA	3.5mA
EIN_STATUS_12	D12	7mA	3.5mA

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The status inputs are detected via analog signals. A digital conversion is done in the unit.

Programming possibilities in the PLC program (allocation editor, parameter editor) for **EIN_STATUS_xx**

- Upper threshold value
- Lower threshold value
- Type (order of the ranges „ON(1)“, „OFF(0)“, „ERROR(E)“)
- Error time (can only be branch generally for each multiplex nodes)

The parameter upper and lower **threshold value** are specified relative to the board voltage in percent (0...100% U_{PLUS}). The range of the board voltage is divided into three areas through the two threshold values.

The **type** parameter specifies, which conditions are allocated to the three areas.

- Area above the upper threshold value (1,0 or E)
- Area in the middle (1,0,E or -)
- Area below the lower threshold value (1,0 or E)

The **error time** parameter specifies the time t after which an error is reported. The time is entered in steps of 10ms in the range of value from 0...250 ($t = 0...2500ms$). The error time is valid for all status inputs of a multiplex node.

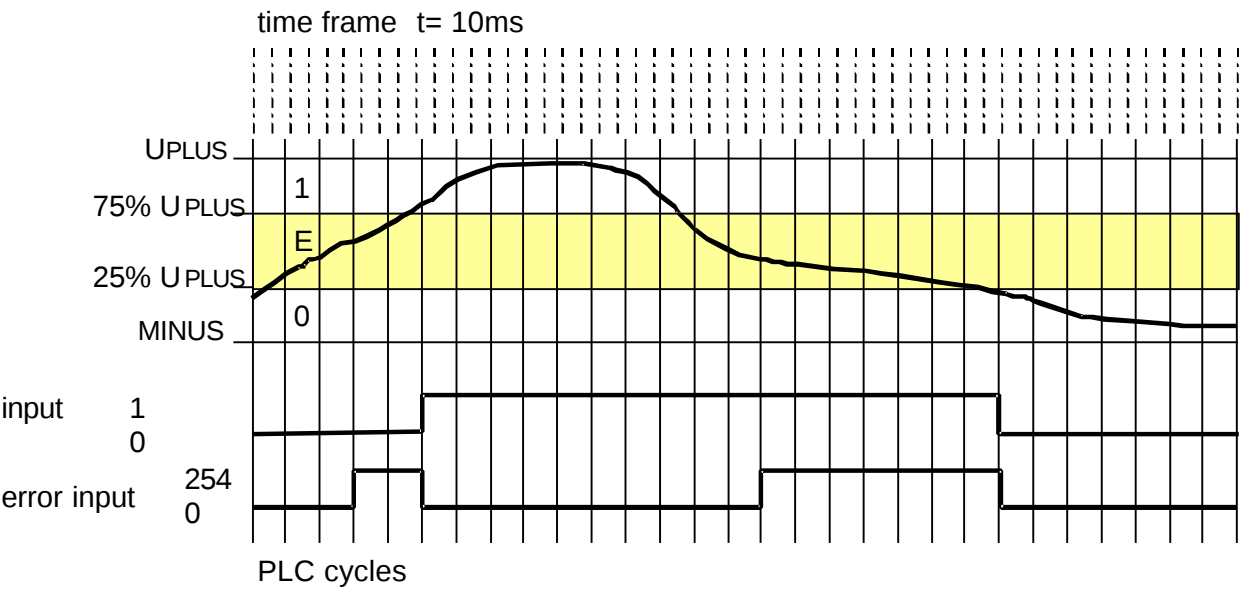
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Examples:
(upper threshold value = 75%, lower threshold value = 25%, board voltage = 24V)

0-1 →	voltages above 18V voltages between 6 and 18V or voltages below 6V	→condition „inactive“ →condition „active“ →condition „inactive“ →condition „active“
01E →	voltages above 18V voltages between 6 and 18V voltages below 6V	→condition „inactive“ →condition „active“ →condition „active error“
1E0 →	voltages above 18V voltages between 6 and 18V or voltages below 6V	→condition „active“ →condition „active error“ →condition „inactive error“ →condition „inactive“

Example: (error time: 3 → t = 30ms)



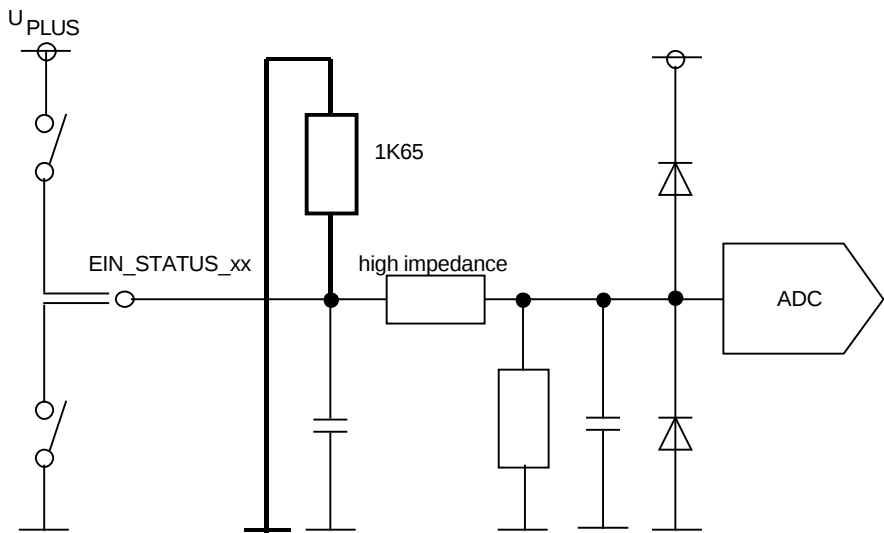
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Note:

The status inputs are supplied to the PLC directly, that means without SW filtering. Interference voltages at the input are effectively suppressed by setting a hysteresis. From the standard setting of the status inputs (lower threshold value 33%, upper threshold value 66%, type 1E0, error time 50(=500ms)), a hysteresis range of 33% U_{PLUS} results (corresponds to the error range in this example). Through the definition of the error time, sporadic error messages are suppressed at the same time (for signals with slow condition change, the error time also prevents the reporting of an error). Additional protection can be programmed with a respective time filter in the PLC program.

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5.5.1.1.1 Characteristics during power down



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5.5.1.2 Analog inputs

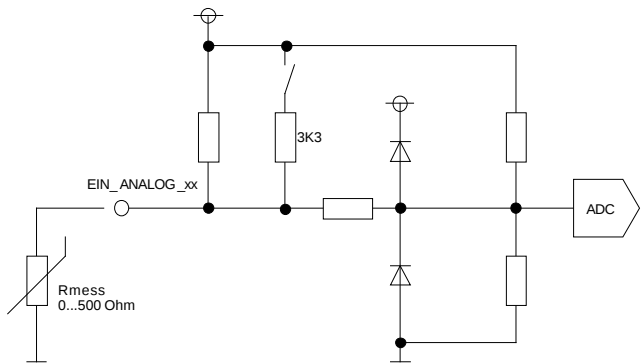
Name	Connector pin
EIN_ANALOG_01	D13
EIN_ANALOG_02	D14

For the analog inputs, there are different measurement methods available.

5.5.1.2.1 Parameter setup

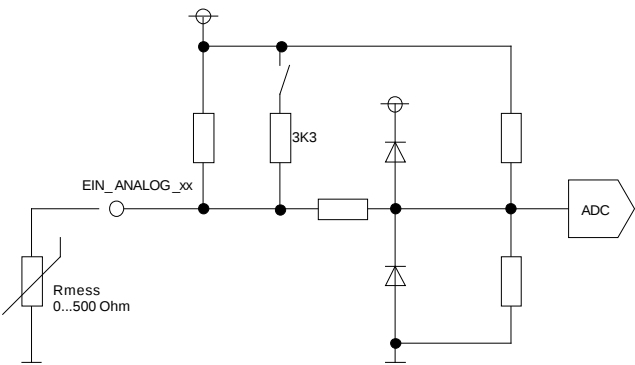
Programming possibilities in the PLC program (allocation editor) for **EIN_ANALOG_xx**

- Type0: **R OFF** **Resistance measurement** in the range 0...500Ω.
 Linear transmission of the measured value, that means consistent resolution over the complete measuring range,
 compensation of a possible **ground offset**.

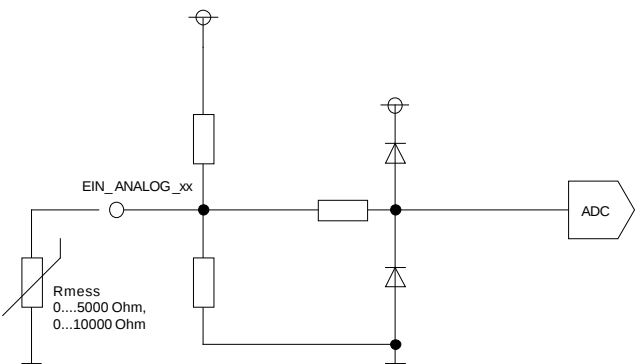


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- Type1 : R **Resistance measurement** in the range 0...500Ω, 0..5000Ω or 0...10000Ω.
Linear transmission of the measured value, that means consistent resolution over the complete measuring range.
no compensation of a possible ground offset.



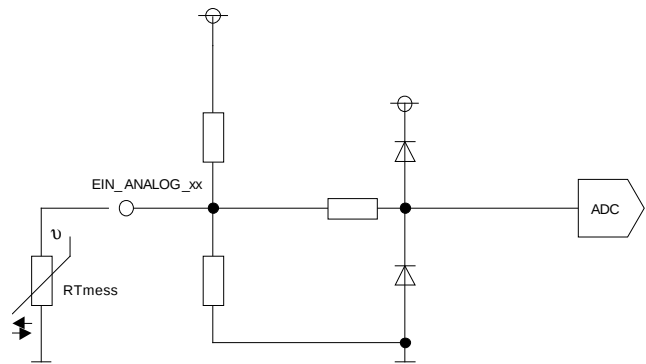
0...500Ω



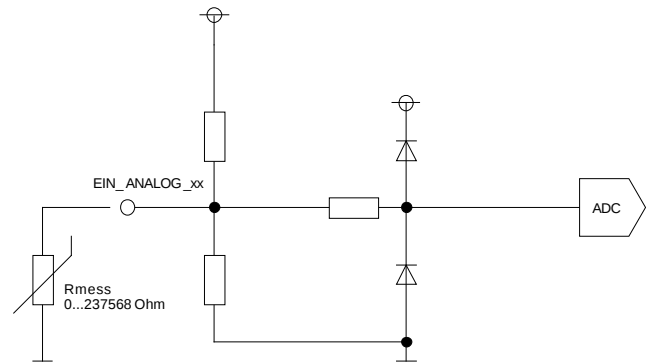
0...5000Ω and 0...10000Ω

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- **Type2 : NTC** **Temperature measurement** via thermal resistor with NTC characteristic, in the range -35...90°C or -40...210°C.
Linear transmission of the measured value, that means consistent resolution over the complete measuring range.
No compensation of a possible ground offset.



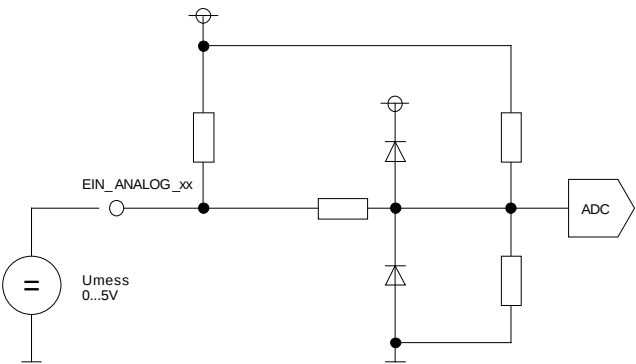
- **Type3 : R n.lin** **Resistance measurement** in the range 0...237568Ω.
Non-linear transmission of the measured value, that means a resolution adjusted in steps to the measured variable.
No compensation of a possible ground offset.



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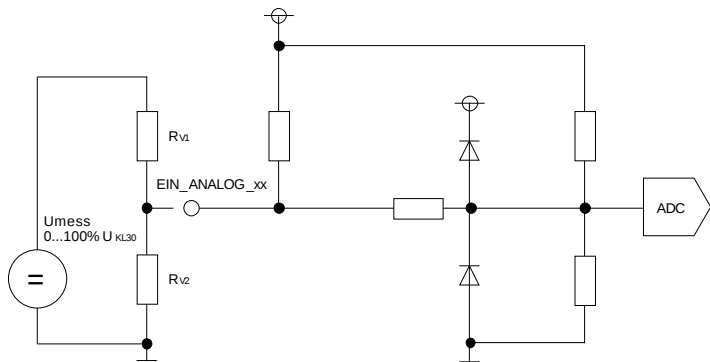
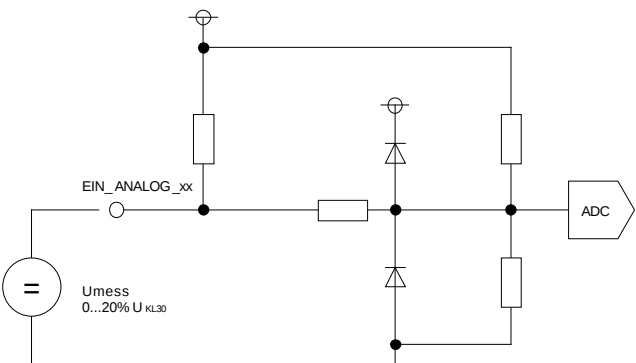
• Type4 : U absolute

Voltage measurement in the range 0...5V.
Linear transmission of the measured value, that means consistent resolution over the complete measuring range.
No compensation of a possible ground offset.



• Type5: U relative **Voltage measurement relative** to U_{PLUS} in the range 0...U_{PLUS} with external voltage divider.

Linear transmission of the measured value, that means consistent resolution over the complete measuring range.
No compensation of a possible ground offset.



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5.5.1.2.2 Specification

	PARAMETER			Measuring range	Resolution	
	Value1	Value2	Value3			
R OFF	0	500	-	0...500Ω	2Ω	
R	0	500	-	0...500Ω	2Ω	
	0	5000	-	0...5000Ω	20Ω	
	0	10000	-	0...10000Ω	40Ω	
NTC	R ₂₅	B value	0.5°C	-35...90°C	0.5°C	
	R ₂₅	B value	1°C	-40...210°C	1°C *)	
$R_T = R_{25} * \exp[B * (1/T - 1/T_0)]$ with To = 298K (25°C)						
R n.lin	-	-	-	0...237568Ω	64Ω for 0Ω ≤ R ≤ 4096Ω 128Ω for 4096Ω ≤ R ≤ 8192Ω 256Ω for 8192Ω ≤ R ≤ 16384Ω 512Ω for 16384Ω ≤ R ≤ 32768Ω 1024Ω for 32768Ω ≤ R ≤ 65536Ω 2048Ω for 65536Ω ≤ R ≤ 131072Ω 4096Ω for 131072Ω ≤ R ≤ 237568Ω	
U absolute	0	5000	-	0...5V	20mV	for U _{PLUS} = 23..32V
				0...2V		for U _{PLUS} = 10..32V
U relative	0	20	-	0...20% U _{PLUS}	0.08% U _{PLUS}	
				0...100% U _{PLUS}	0.4% U _{PLUS}	with ext. voltage divider R _{V1} = 5K6 and R _{V2} = 1K5

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*) In the PLC program, all analog values are processed in the range 0..500. However, the resolution is determined by the transmission. The transmission takes place in the range 0...250. The analog value changes by 2 digits/resolution (500/250 = 2 digits). In the measuring range -40...210°C, the analog value changes by 2 digits/1°C.

Example:

Analog value	0	→	T = -40°C
Analog value	2	→	T = -39°C
	:		
Analog value	100	→	T = +10°C
Analog value	498	→	T = +209°C
Analog value	500	→	T = +210°C

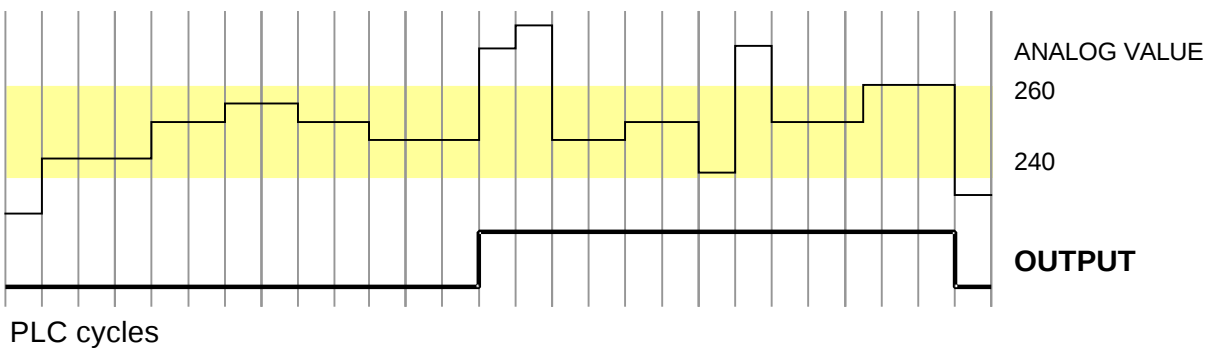
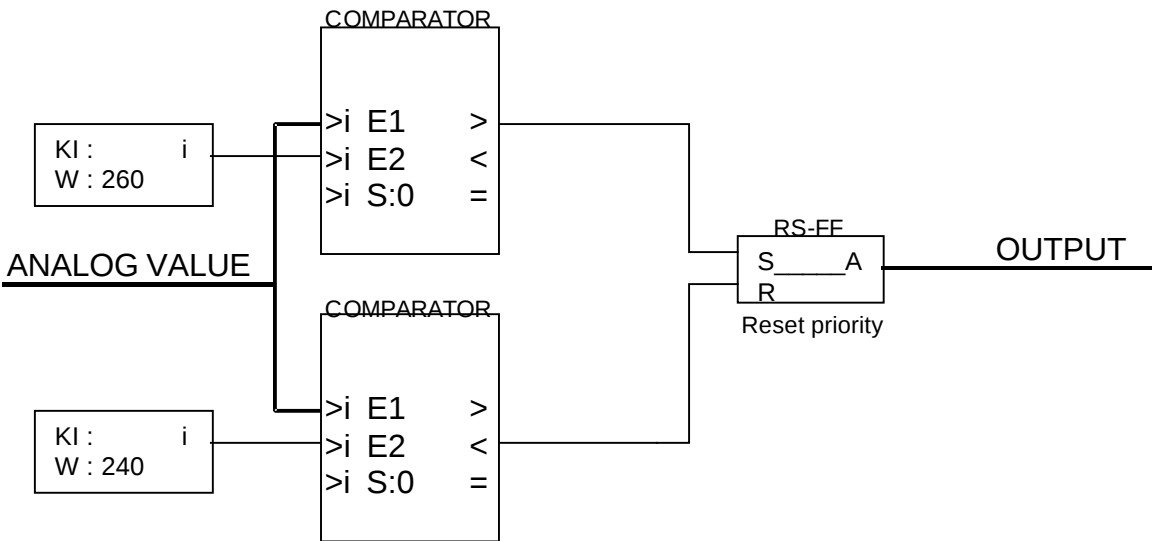
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Note:

The analog inputs are directly provided to the PLC, which means without SW filtering. For the display of analog values, for example as bar graph, the use of an average value module is generally recommended in the PLC program. For the monitoring of the threshold value of analog values, an average value module is recommended as well and/or the use of a comparator with programmable hysteresis (s. example 1). Exceeding the threshold value for a short time can also be suppressed by a edge delay module (see example 2).

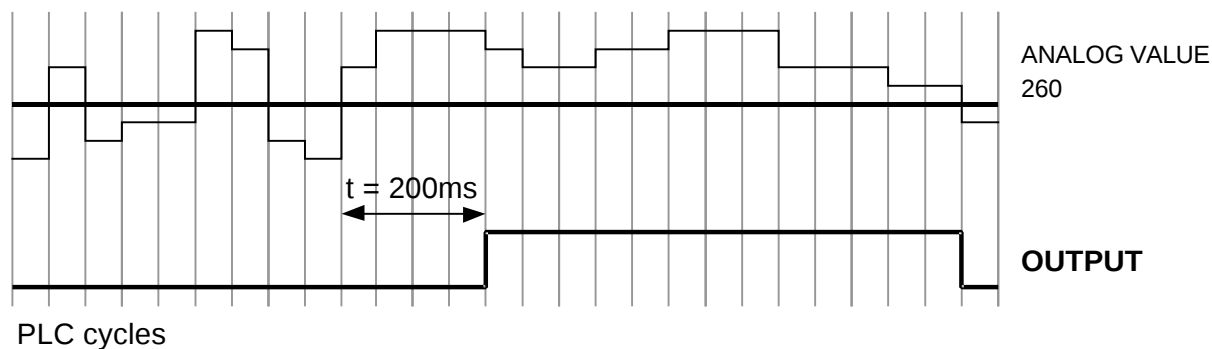
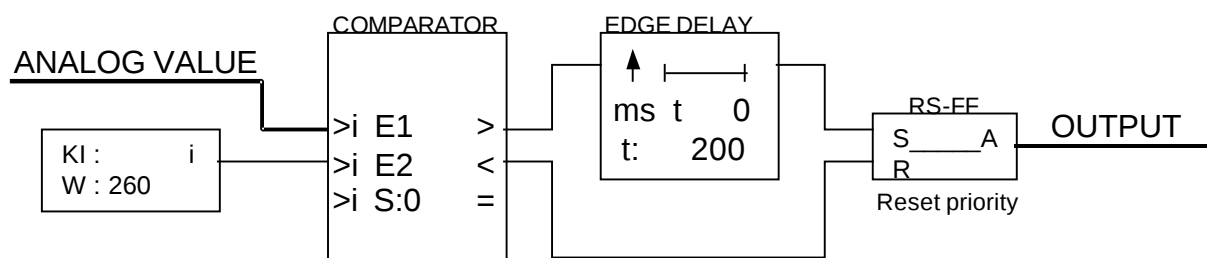
Example 1 :

Monitoring of the threshold value of an analog value (250) by a window discriminator with a hysteresis range of 20 (between the analog values 240 and 260).



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Example 2 :
Brief deviations from the threshold value are filtered by a edge delay module. With an additional edge delay module, resetting of the output can be filtered as well.



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5.5.2 Outputs

For wiring, use cables approved for automotive usage with a minimum nominal wire cross-section of 1mm².

At least 2.5mm² are recommended for the power supply PLUS_Gx and Minus.

Voltage drop, load current and heating have to be taken into account when specifying the wire cross-section.

Use the tinned or silver-plated "Junior Power Timer" contact by Tyco (AMP). Following types of contacts are available:

Tyco (AMP) order no. according to cross section:

1.0 mm ²	2,5 mm ²	Material / contact
927 771-3	927 768-3	CuSn4 / pretinned
927 771-1	927 768-1	CuFe2 / pretinned
927 771-6	927 768-6	CuSn4 / presilvered

The theoretical overall switching current of the multiplex node amounts to 52A.

IMPORTANT : For thermal reasons, the switching current available at the same time is in the "worst case" **max. 25A** (full load, based on the upper limit of the supply voltage range of U = 16V or U = 32V).

„Worst case“ means that few outputs are operated with the max. admitted switched current. The occurring power dissipation quadruples with the switching current ($P_V = I^2 \cdot R_{DS(on)}$). This means if the switched current of an output is reduced by 10%, the power dissipation is reduced by 19% ($0.9^2 = 0.81$)

This means that the switching current available at the same time increases by 10%, if the switching currents admitted in each case are only utilized by 90%.

Example: Instead of 8 x 3A, 10 x 2.7A can be switched.

Within one supply group (group 1 or 2) a max. of 15A may be switched. The supply groups have to be fused with a max. of 15A each.

To protect the circuit of the LS-loads, group 1 (PLUS_G1) must be fuse protected.

	Name	Connector pin	Note
Group 1	PLUS_G1 MINUS_G1	A1 A2	Fusing via 15A
Group 2	PLUS_G2 MINUS_G2	A3 A4	Fusing via 15A

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5.5.2.1 HIGHSIDE - switch

	Name	Connector pin	Switching current	Note
Group 1	AUS_01_G1_HS	B21	3A	Circuit protection via ext. 15A fuse
	AUS_02_G1_HS	B19	3A	
	AUS_03_G1_HS	B15	3A	
	AUS_04_G1_HS	B13	3A	
	AUS_05_G1_HS	B9	3A	
	AUS_06_G1_HS	B7	3A	
Group 2	AUS_09_G2_HS	E1	3A	Circuit protection via ext. 15A fuse
	AUS_10_G2_HS	E3	3A	
	AUS_11_G2_HS	E5	3A	
	AUS_12_G2_HS	E7	3A	
	AUS_13_G2_HS	E11	3A	
	AUS_14_G2_HS	E13	3A	
	AUS_15_G2_HS	E15	3A	
	AUS_16_G2_HS	E17	3A	

Special case:

A maximum of 7 outputs of the 14 outputs may be operated with 3.5A.

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By connecting (jumper to the connector) of 2 outputs, the switching current can be increased. The open-load recognition in the on-condition is not possible any more for parallel connections.

It is not allowed to supply the same load with HS-outputs of different groups, because the separate groups shall also be fuse protected separately.

The connection has to be done within the same group with neighboring channels.

For example:

AUS_01_G1_HS + AUS_02_G1_HS,
AUS_03_G1_HS + AUS_04_G1_HS, etc.

Take care, that the output pins don't get current from outside.

5.5.2.1.1 Parameter setup

Programming possibilities in the PLC program (allocation editor) for **AUS_xx_G1_HS**

- **„fail safe“ operation**
A: output turned off
E: output turned on
H: maintain condition
B: output flashes

- **OpenLoad in ON**

For the open-load recognition in the on-condition, the power switch is turned off for $t = 1\text{ms}$.

- **Overload latch**

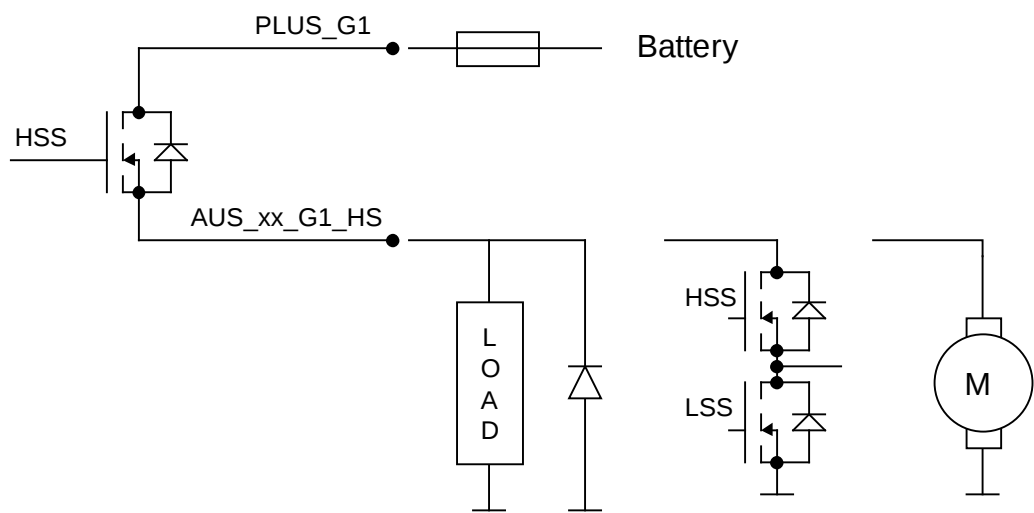
With activated “overload latch”, the HSS output remains switched off after detection of an overload until it is switched on again by ZR2. At “overload latch = off”, the output remains switched on logically, if it is not switched off by ZR2. During this time, the output will automatically switched on again but thermally controlled.

In both cases, the output transmits an error message to ZR2. In general, the PLC program should be structured such that the error messages are evaluated. This is especially important in case of frequently or periodically controlled outputs (e.g. for flash indicator applications) because otherwise an output may always be short-circuited despite activated “overload latch”.

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5.5.2.1.2 Specification : Reverse battery protection

At reverse battery protection the HSS are sufficiently protected for a short time through the load.
However, in special cases there is no reverse battery protection through the external wiring.
For example: - the load has an integrated or external freewheeling diode
- the load consists of an MOSFET- half bridge (for example HSS, LSS)
- a connected motor does block and the load current is no more limited



In addition it has to be taken into account that certain loads have to be reverse battery protected themselves.
For example: - electronic components, valves
- a motor that may not to be turned in the wrong direction

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5.5.2.1.3 Specification : Diagnosis

	Input level	Status
Normal operation	Turned off	O.K.
	Turned on	O.K.
Short circuit to ground (clean short circuit ¹⁾)	Turned off	O.K.
	Turned on	Error
Overtemperature	Turned off	O.K.
	Turned on	Error
open load	Turned off	Error
	Turned on	O.K.
	Turned on	Error ³⁾

¹⁾ Short circuit to ground:
(typ. values)

short circuit current = 30A for t < 3ms

The short circuit and excess temperature protection is done via the power dissipation occurring in the component, which leads to a temperature increase and therefore to a shut-off.

If the "overload latch" is inactive, the subsequent cooling leads to repeated turning on at lower short circuit currents.

With activated overload latch, the HSS output remains switched off after detection of an overload until it is switched on again by ZR2.

The short circuit operation may trip or damage the external fuse.

²⁾ open-load recognition for ohmic loads.

This function has to be enabled in the allocation editor.

For the open-load recognition, a pull-up resistor with 330 kΩ is connected to Plus_Gx for each output. Take this into account for high-impedance loads with regard to output voltage in off-condition.

For the open-load recognition in the on condition, the power switch is turned off for t = 1ms.

The open-load recognition of the individual outputs is done with different time offset. Therefore no open-load recognition is possible in the on-condition when connecting (jumper at the connector) 2 outputs in parallel.

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5.5.2.1.4 Specification : Inductive loads

E_{AS} : energy absorbed by the PROFET when an inductive resistor is switched off.

$$E_{AS} < 0.28 \text{ J (3A switch)}$$

The specification is valid for pure inductive loads (for example relay).

At direct-current motors it also has to be taken into account that they change to generator operation when turned off and that they return energy.

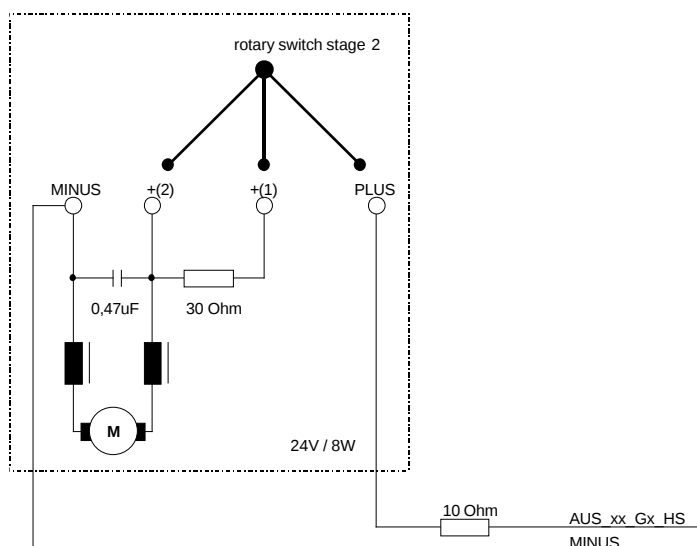
In applications with direct-current motors, which are not switched directly via the HSS but via a mechanical contact (for example: fan with integrated 2-stage rotary switch), additional protection measures may be required (external series resistor). These protection measures are necessary in particular, if the direct-current motor has an integrated interference-suppression capacitor. The resulting parallel LC- oscillating circuit in connection with the spark-discharge gap at the contact can lead to extreme current and voltage peaks.

However, these protection measures are application specific and only practical for motors with low power consumption due to power dissipation. Through the series resistor, the supply voltage of the direct-current motor is reduced, too.

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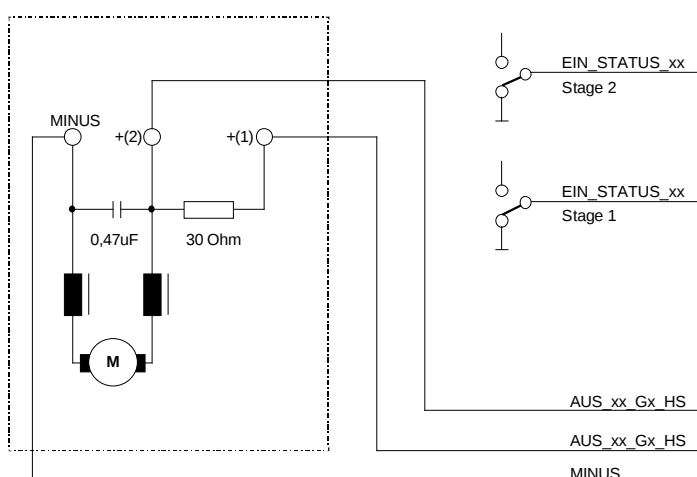
Product description

Example:



In general, the direct control of each stage with one HSS each has to be given preference in these cases.

Example:



5.5.2.2 LOWSIDE - switch 3A

	Name	Connector pin	Switching current Power switch	Note
Group 1	AUS_07_G1_LS AUS_08_G1_LS	B3 B1	3A 3A	Circuit protection via ext. user protection

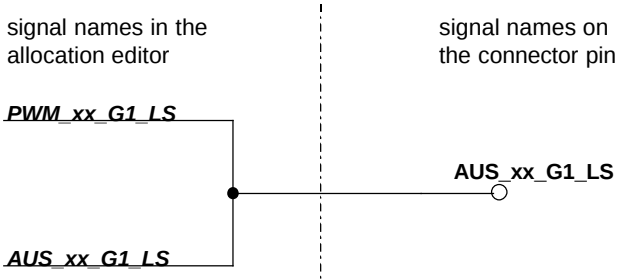
To protect the circuit of the LS-loads, group 1 (PLUS_G1) must be fuse protected.

The outputs can be configured in various modes with different output stages. All outputs have a low-impedance power switch.

The power switch can be operated as switch output (*AUS_xx_G1_LS*), PWM – output (*PWM_xx_G1_LS*) or MONOFLOP – output (*PWM_xx_G1_LS*). During switch and Monoflop mode, the switching-on of the LS power switch is delayed by $t = 1\text{ms}$ relative to the PLC cycle.

The logic switch can be operated as PWM – output (*PWM_xx_G1_LS*) or MONOFLOP – output (*PWM_xx_G1_LS*). During the Monoflop mode, the switching-on of the logic switch is delayed by $t = 1\text{ms}$ relative to the PLC cycle.

AUS_xx_G1_LS and *PWM_xx_G1_LS* are using a common connector pin (*AUS_xx_G1_LS*). This means that the *AUS_xx_G1_LS* should not be allocated or turned off for the PWM / MONOFLOP – function.

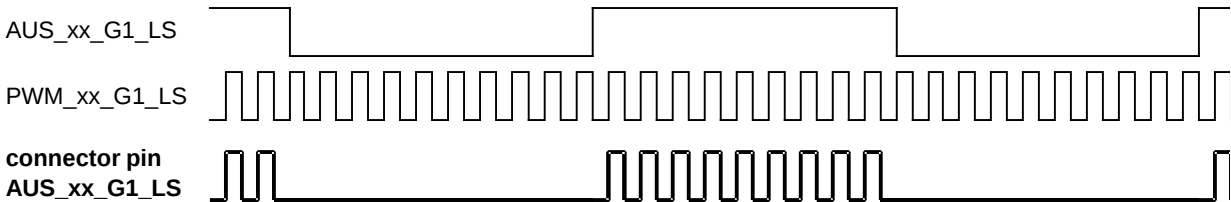


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Note:
The outputs *AUS_xx_G1_LS* and *PWM_xx_G1_LS* are operated in parallel (according to the definitions in the allocation editor and the PLC program).
This means that the outputs are connected by a logic OR in normal operation as well as during „fail safe“ operation.

- Example:
- „fail safe“ operation B: output flashes (*AUS_xx_G1_LS*)
 - „fail safe“ operation N: take over „fail safe“ operation value (125) (*PWM_xx_G1_LS*)

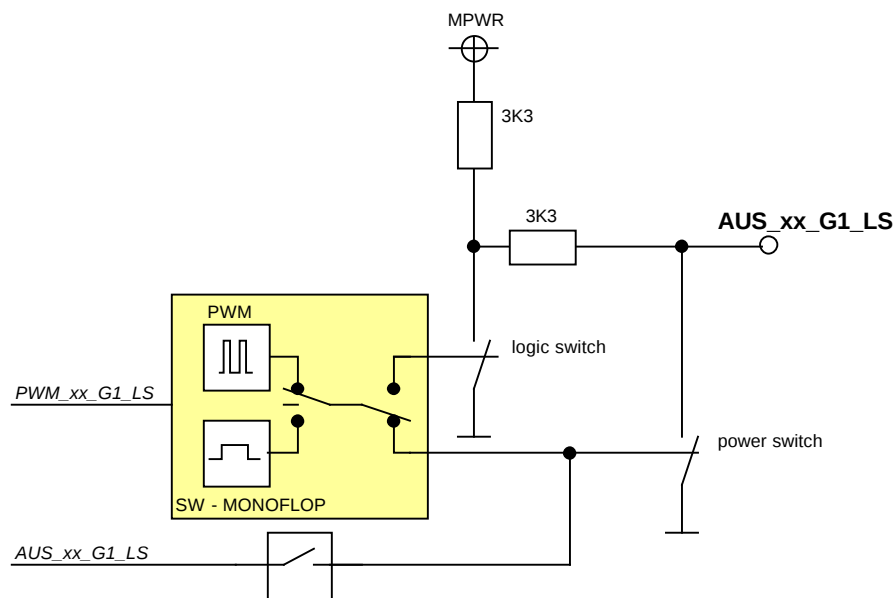
The result of this „fail safe“ operation definition is the following signal curve at the output.



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5.5.2.2.1 Parameter setup

- ◆ The outputs can be operated as *AUS_xx_G1_LS* or as *PWM_xx_G1_LS* (PWM, SW-MONOFLOP). The basic PWM frequency is the same for all outputs.



Programming possibilities in the PLC program (allocation editor) for:

AUS_07_G1_LS, AUS_08_G1_LS

- **„fail safe“ operation**
 - A: output turned off
 - E: output turned on
 - H: maintain condition
 - B: output flashes
- **OpenLoad in ON** For the open-load recognition in the on condition, the power switch is turned off for $t = 1\text{ms}$. The diagnosis for the power switch is only available, if the output *PWM_xx_G1_LS* is not allocated.

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PWM_07_G1_LS, PWM_08_G1_LS

For the Monoflop / PWM – function the *AUS_xx_G1_LS* should not be allocated or turned off.

- **Type1 : PWM-output at power switch**

PWM signal on power switch. For EMC reasons the control of peripheral equipment (for example fans) has to be given preference over the logic switch.

- „fail safe“ operation

H: maintain condition

N: take over „fail safe“ operation value (PWM)

- **Type2 : PWM-output at logic switch**

PWM signal on logic switch.

- „fail safe“ operation

H: maintain condition

N: take over „fail safe“ operation value (PWM)

- **Type3 : Monoflop on power switch**

With each PLC cycle the power switch is turned on for $t = 0..250\text{ms}$. The output remains active at $t > T_{\text{ZYKLUS}}$, but is switched off during each PLC cycle for 1 ms.

- „fail safe“ operation

A: output turned off

- **Type4 : Monoflop on logic switch**

With each PLC cycle the logic switch is turned on for $t = 0..250\text{ms}$. The output remains active at $t > T_{\text{ZYKLUS}}$, but is switched off during each PLC cycle for 1 ms.

- „fail safe“ operation

A: output turned off

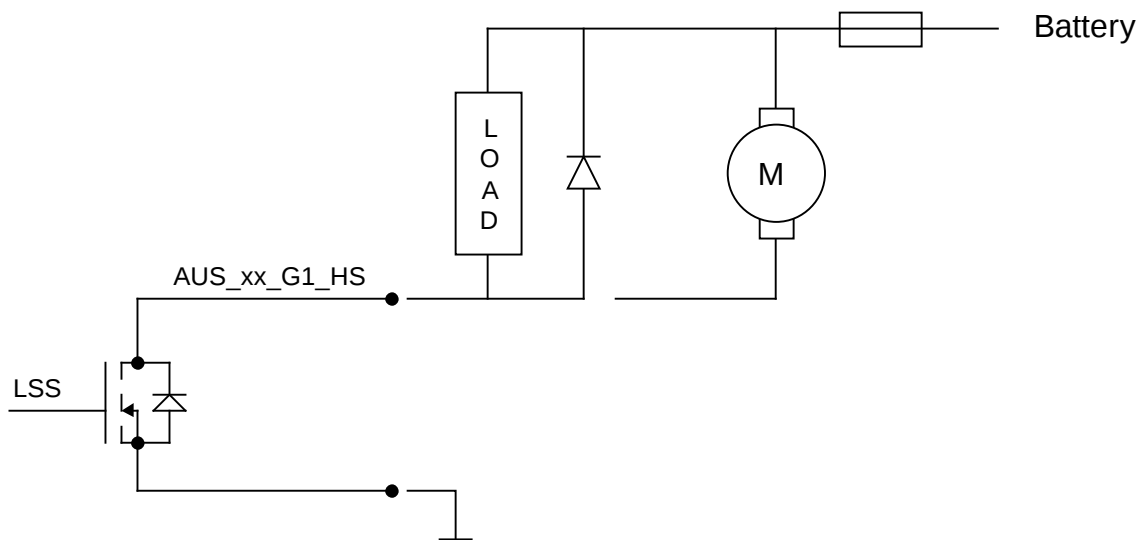
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5.5.2.2.2 Specification LOWSIDE - switch

SELECTION	Parameter		Current	Note
in the PLC program	T _{ON}	Frequency		
AUS_xx_G1_LS			3A	
OpenLoad in ON				
PWM_xx_G1_LS				
PWM-output at power switch	0...100%	20... 30000Hz	3A	Resolution(T _{ON}) = 1/250%
PWM-output at logic switch	0...100%	20... 30000Hz	R _{IL} = 3K3 R _{IH} = 6K6	Resolution(T _{ON}) = 1/250%
Software monoflop at power switch	0...250ms	-	3A	
Software monoflop at logic switch	0...250ms	-	R _{IL} = 3K3 R _{IH} = 6K6	

5.5.2.2.3 Specification : Reverse battery protection

At reverse battery protection the LSS are sufficiently protected through the load for a short time.
However, in special cases there is no reverse battery protection through the external wiring.
For example: - the load has an integrated or external freewheeling diode
- a connected motor does not block and limit the load current any more



In addition it has to be taken into account that certain loads have to be reverse battery protected themselves.
For example: - electronic components, valves
- a motor that may not to be turned in the wrong direction

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5.5.2.2.4 Specification : Diagnosis

The diagnosis for the power switch is only available, if the output *PWM_xx_G1_LS* is not allocated.

	Input level	Status
Normal operation	Turned off	O.K.
	Turned on	O.K.
Short circuit to ground	Turned off	Error
	Turned on	O.K.
Short circuit to V_{bb}	Turned off	O.K.
	Turned on	Error ¹⁾
Overtemperature	Turned off	O.K.
	Turned on	Error
open load	Turned off	Error
	Turned on	O.K.
	Turned on	Error ²⁾

¹⁾ short circuit to V_{bb} is recognized via the power dissipation occurring in the component

²⁾ open-load recognition for ohmic loads.

This function has to be enabled in the allocation editor.

For the open-load recognition in the on condition, the power switch is turned off for $t = 1\text{ms}$.

The open-load recognition of the individual outputs is done with different time offset.

Therefore no open-load recognition is possible in the on-condition when connecting (jumper at the connector) 2 outputs in parallel.

The short circuit and excess temperature protection is done via the power dissipation occurring in the component, which leads to a temperature increase and therefore to a shut-off.

An error message is displayed and the output remains switched off until it is switched on again by ZR2.

However, in the PWM mode, the LSS is switched on periodically so that no long term short circuit protection is given.

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I _{SHORT CIRCUIT}	t _{SHORT CIRCUIT}	U _{BAT}	Note
80A	375µs	28V	with R _{LOAD} = 0Ω
28A	10ms	28V	with R _{LOAD} = 1Ω

The data are typical values at room temperature.

5.5.2.2.5 Specification : Inductive loads

E_{AS}: energy that the LSS absorbs when an inductive resistor is switched off.

E_{AS} < 0.2 J

The specification is valid for pure inductive loads (for example relay).

At direct-current motors it also has to be taken into account that they change to generator operation when turned off and that they return energy.

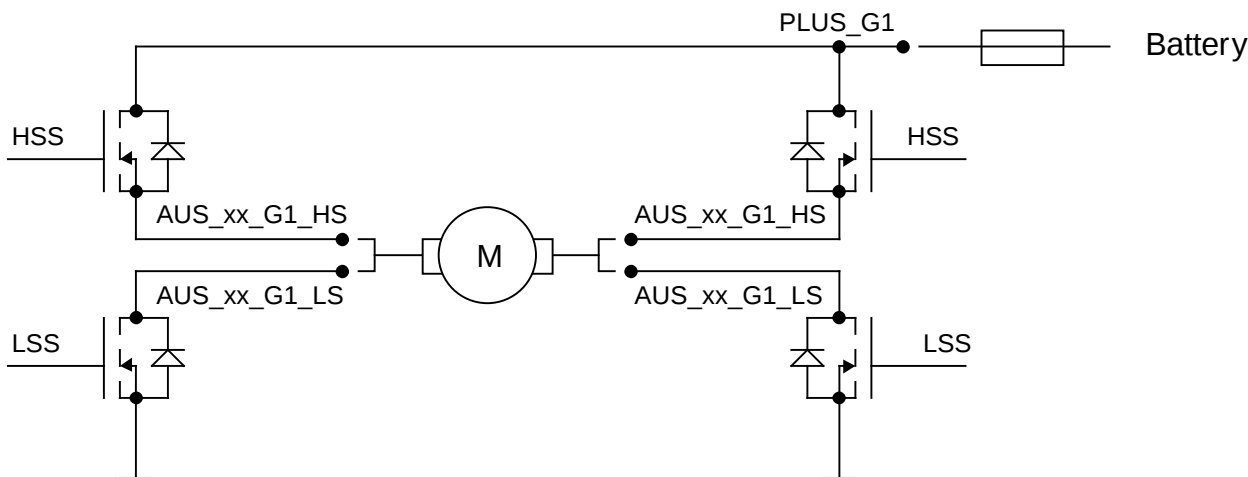
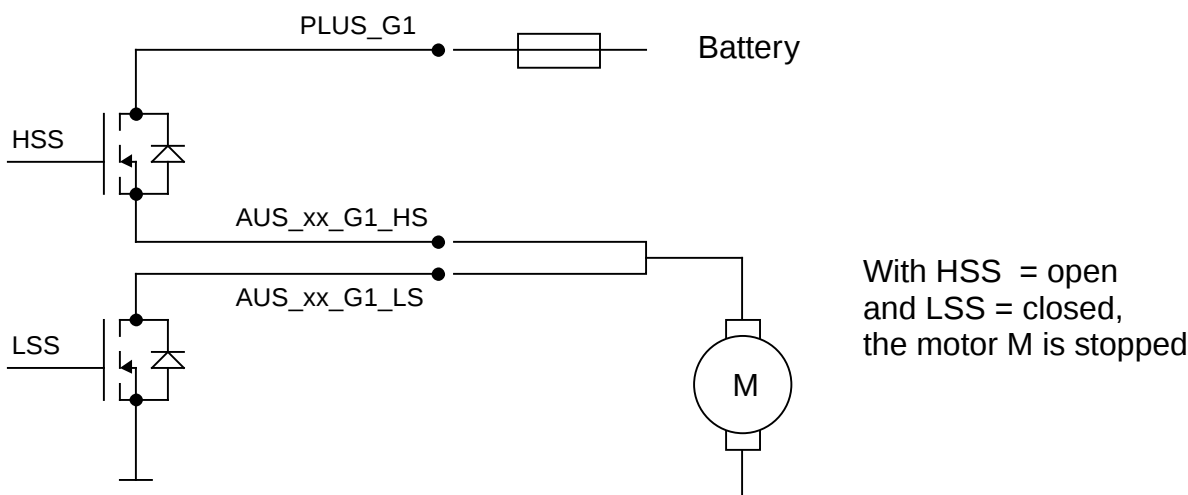
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5.5.2.3 HALF BRIDGES 3A

By connecting (jumper at the connector) of a HSS and a LSS a half-bridge is formed.

The half-bridges are formed with HSS and LSS of group 1. Simultaneous switching-on of LSS and HSS must be avoided within the PLC program.
The switching-on of the LSS is delayed by $t = 1\text{ms}$ with regard to the PLC cycle (and herewith, to the HSS) in order to avoid cross currents due to different switch delay times.

The half-bridges (and full-bridges) are not sufficiently reverse battery protected by the external fuse at the PLUS - side!

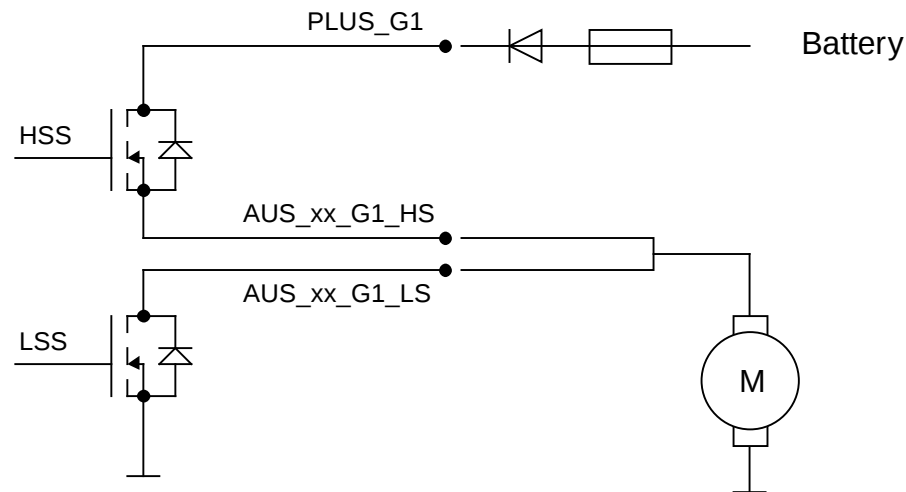


A full-bridge consists of 2 half-bridges. They can control the direction of rotation of a motor M for example.

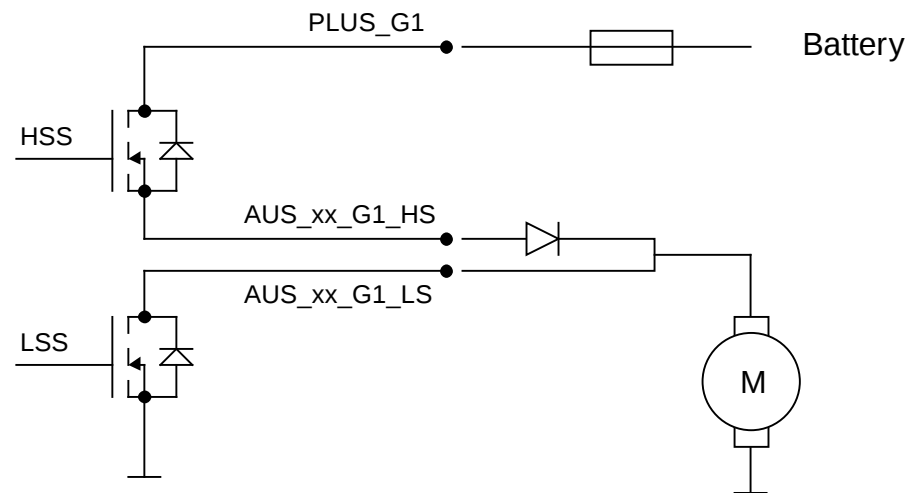
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External measures are necessary to protect the outputs.

- An external diode (preferably Schottky diode) in the voltage supply prevents the current flow. The diode operated by the current of the whole group and therefore has to be designed appropriately (current, power dissipation).



- An external diode at the output of the respective HB has the advantage, that not the complete group current is lead through the diode.

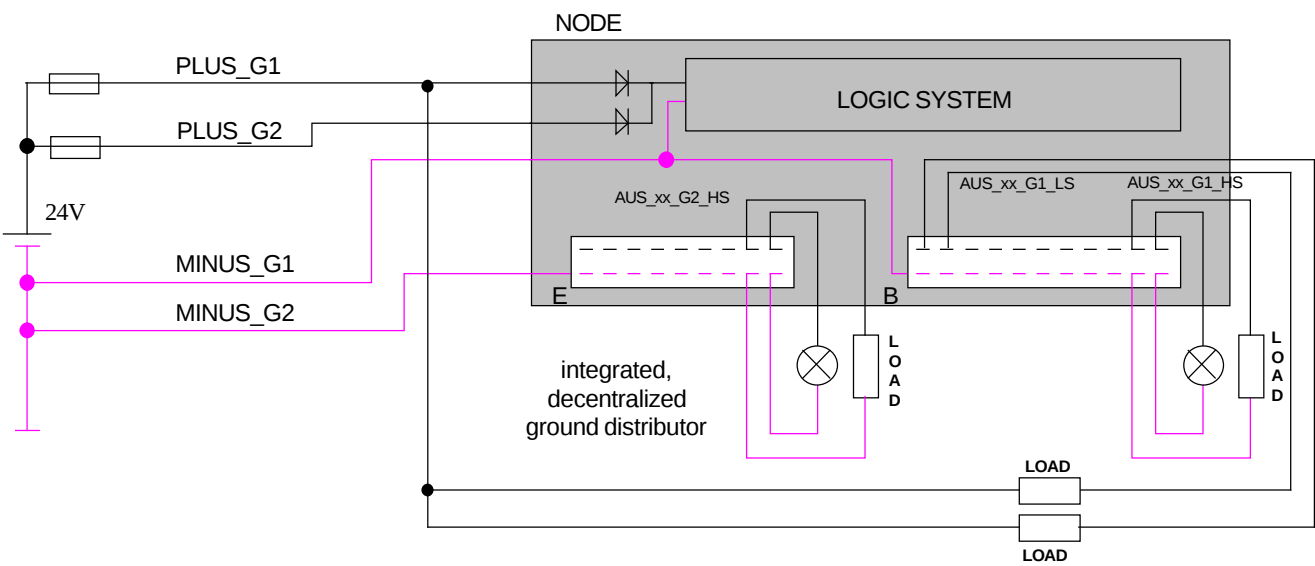


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5.5.2.4 Ground neutral point

	Name	Connector pin	Note
Group 1	MINUS_G1	A2	Ground supply
	MINUS_G1	B4	
	MINUS_G1	B4	
	MINUS_G1	B6	
	MINUS_G1	B8	
	MINUS_G1	B10	
	MINUS_G1	B12	
	MINUS_G1	B14	
	MINUS_G1	B16	
	MINUS_G1	B18	
	MINUS_G1	B20	
	MINUS_G1	B22	
Group 2	MINUS_G2	A4	Ground supply
	MINUS_G2	E4	
	MINUS_G2	E4	
	MINUS_G2	E6	
	MINUS_G2	E8	
	MINUS_G2	E10	
	MINUS_G2	E12	
	MINUS_G2	E14	
	MINUS_G2	E16	
	MINUS_G2	E18	

The ground neutral point of each group is designed for 15A.
To operate the multiplex node MINUS_G1 is necessary.



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